2020

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IEEE

Tencate, Timothy, Giovanna Oriti, and Alexander Julian. "Comparison of Control Methods for Single-Phase Inverters to Meet the Requirements in IEEE Standard 1547-2018." 2020 IEEE International Conference on Environment and Electrical Engineering and 2020 IEEE Industrial and Commercial Power Systems Europe (EEEIC/I&CPS Europe). IEEE, 2020.

http://hdl.handle.net/10945/65809

Comparison of Control Methods for Single-Phase Inverters to Meet the Requirements in IEEE Standard 1547-2018

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***Abstract*— This paper compares the performance of different control strategies for a single-phase inverter interfacing a distributed energy resource during abnormal transients or failures of the utility electric power system voltage. The performance of the various control methods is presented and compared to IEEE Standard 1547-2018 using a physics-based model. The simulation scenarios are created to compare the controller responses to the intentional island and ride-through recommended timing specified in IEEE Standard 1547-2018. The physics-based model is validated by experimental measurements on a laboratory prototype with a Field Programmable Gate Array - based controller.**

Keywords—distributed energy resource, grid disconnection, ride-through, IEEE Standard

I. INTRODUCTION

Distributed energy resources (DERs) connected to local area electrical power systems (LAEPS) have recently grown in number due to the increased demand for local power availability and energy security. When disturbances or faults occur in the utility electric power system (EPS), DERs can keep local critical loads serviced, thus increasing the energy security of a LAEPS. IEEE Standard 1547-2018 [1] provides guidelines for the connection of a DER to the utility EPS, also known as the main AC grid. This standard requires that the DER control system has a quick enough response time to ensure that other DERs and loads are not affected by the transient when switching from grid connected mode to intentional islanding mode. It also requires that a DER maintains connection for a specified time, known as voltage ride-through time, during allowable voltage disturbances in the utility EPS voltage.

Although much literature exists on control methods for grid-interfacing inverters, the performance of their controller has not been previously compared to the requirements of [1]. Reference [2] includes an overview and comparison of the prevalent Phased Locked Loop (PLL) techniques for the design of grid-connected inverter systems. In [3] four different orthogonal generation methods (OGMs) for single phase inverters were explored and tested extensively, pointing to the most effective OGM to support synchronous reference frame controllers. Reference [4] presents a simple peak-detection method for a single-phase inverter to transition to island operation when a grid failure occurs. In [5] two dual second order generalized integrators were used in conjunction with a combination of overvoltage, under voltage, over frequency, and under frequency trip points to determine an inverter's connection to the utility EPS. The grid connection method presented in [5] was based on the research presented in [6] where multiple second-order generalized integrators (MSOGIs) and their effectiveness under distorted grid conditions were analyzed. It also presented methods for tuning the MSOGIs to different frequencies to achieve selective and adaptive filters working in parallel. This method is very accurate but more complex from a computational perspective.

This paper reviews and compares the control methods presented in [2]-[6] with respect to the recommendations in IEEE Standard 1547-2018 for islanding and ride-through operations of a DER connected to the utility EPS through a single-phase inverter. To these authors' knowledge, such a thorough study of the standard has not been presented in previous literature. Furthermore a novel detection and islanding control method is presented, which combines accurate response and simplicity. A physics-based model was developed and experimentally validated for this research.

This paper is organized as follows; first the system architecture is defined in section II together with an overview of the abnormal voltage requirements in IEEE Standard 1547-2018, then the various control methods are presented in section III. Section IV includes simulation results comparing the performance of the different controllers with respect to IEEE Standard 1547-1800. The physics-based model used for this research is experimentally validated in section V and the conclusions are presented in section VI.

II. SYSTEM ARCHITECTURE AND IEEE STANDARD

The power system in Fig. 1 includes a DER with a DC bus and a single-phase H-bridge inverter interfacing to the utility EPS through an LC filter. Examples of DERs can be a photovoltaic source, a fuel cell or an energy storage element requiring a DC/DC converter which regulates the DC bus. The inverter operates in current-mode control when it is grid-connected and in voltage-mode control when it is islanded from the grid. In this paper we focus on the control methods that can be implemented when the inverter is operating in current-mode control, while grid-connected and specifically during abnormal operating performance of the EPS voltage.

IEEE Standard 1547-2018 [1] regulates the interconnection of DERs to the area EPS, including cases of abnormal operation of the EPS. The focus of this paper is unscheduled intentional islanding, which is "formed autonomously from local detection of abnormal conditions at

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the interconnection(s) with the Area EPS, and then automatic relay action that triggers switching action to isolate the intentional island rapidly from the Area EPS", as defined by [1]. The key difference between intentional islanding and unintentional islanding is that the first is a scheduled or unscheduled energization of a planned portion of the local grid that is solely energized by a combination of DER whereas the second occurs when a breaker or other fault detecting equipment isolates a portion of the local EPS, but at the PCC a DER is still energizing a portion of the local EPS, not isolated by the protective device. Unintentional islands must be avoided because it can result in damage to equipment and injury to personnel; "For an unintentional island in which the DER energizes a portion of the Area EPS through the PCC, the DER shall detect the island, cease to energize the Area EPS, and trip within 2 s of the formation of an island" [1].

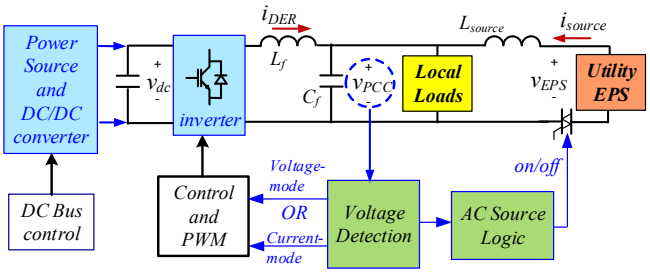

Fig. 1. DER architecture and grid interface.

In this paper we evaluate and compare how different control strategies for the single-phase inverter respond to the area EPS abnormal conditions, as defined in section 6 of [1]. Specifically IEEE Standard 1547-2018, section 6, defines the conditions in which a DER is required to ride-through and those in which it should disconnect from the utility EPS. Ride-through is the "ability to withstand voltage or frequency disturbances inside defined limits and to continue operating as specified" [1]. For Category I systems (common usage, limited penetration of DER), the relevant "shall trip" abnormal voltage conditions are reported in Table I and the ride-through voltage conditions are reported in Table II. Clearing time in Table I is defined as "the time between the start of an abnormal condition and the DER ceasing to energize the Area EPS. It is the sum of the detection time, any adjustable time delay, the operating time plus arcing time for any interposing devices (if used), and the operating time plus arcing time for the interrupting device (used to interconnect the DER with the Area EPS)." [1]

TABLE I. DER RESPONSE (SHALL TRIP) TO ABNORMAL VOLTAGES [1]

Shall trip function	Voltage (p.u. of nominal voltage)	Clearing time (s)
Overvoltage 1	1.20	0.16
Overvoltage 2	1.10	2.0
Undervoltage 1	0.70	2.0
Undervoltage 2	0.45	0.16

To evaluate the transient response of different islanding control methods a physics-based model of the system in Fig. 1 was developed and implemented in Matlab/Simulink using Specialized Power Systems components [7]. The load includes a combination of resistors and inductors as well as a diode rectifier to simulate non-linear loads. The utility EPS was modeled by adding four sine waves; the fundamental with amplitude 110* √2, and 60 Hz, then the 5th, 7th, and 11th harmonics of the fundamental were added with amplitudes as measured in the laboratory. The accuracy of this model was experimentally verified and the relevant measurements are shown in section V.

TABLE II. VOLTAGE RIDE-THROUGH REQUIREMENTS [1]

Voltage range (p.u.)	Operating mode /Response	Minimum ride-through time (s) (design criteria)
V>1.20	Cease to energize	N/A
1.175 < V ≤1.20	Permissive operation	0.2
1.15 < V ≤1.175	Permissive operation	0.5
1.10 < V ≤1.15	Permissive operation	1
0.88 ⩽ V ⩽ 1.10	Continuous operation	Infinite
0.70 ⩽ V < 0.88	Mandatory operation	Linear slope
0.50 ⩽ V < 0.70	Permissive operation	0.16
V < 0.50	Cease to energize	N/A

III. VOLTAGE DETECTION AND RIDE-THROUGH

In this section we present and compare four different control methods for the single phase inverter operating in grid-connected mode. We introduce the disconnection parameter, which gives a measure of each method's ride-through performance. Table II lists the voltage ride-through requirements for abnormal operating performance and section 8.2.4 of IEEE Standard 1547-2018 states: "An intentional island may disconnect from the Area EPS and transition to intentional island mode if any of the trip conditions described in Clause 6 are met (i.e. where Clause 6 would allow or mandate tripping, the intentional island may transition to intentional island mode)" [1].

The above requirements are used to set up the simulation scenarios presented in this paper, which are the basis for comparison of the four voltage detection and ride-through methods described below [8].

1) Peak Detection Method: This method [4] requires little computation yet introduces only a small error, as demonstrated by the experiments presented in section V. Fig. 2 shows the algorithm used to calculate the disconnection voltage v_{dsc} which is then compared to a threshold to determine whether the inverter should stay grid-connected or transition to islanding mode of operation. The gain factor of $\pi/2*\sqrt{2}$ allows the calculation of the RMS value when the input voltage v_{PCC} is a sine wave and α is small.

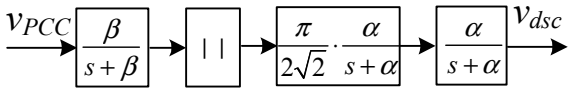

Fig. 2. Peak detection method.

2) DQ-Frame Method: This method, presented in Fig. 3, is based on the transformation of the PCC voltage from the αβ stationary reference frame to the synchronous dq frame with a phase locked loop (PLL) used to track the phase of the voltage. Because the system analyzed is single phase, the orthogonal component of the voltage was generated using a

second order generalized integrator (SOGI), as recommended in [3].

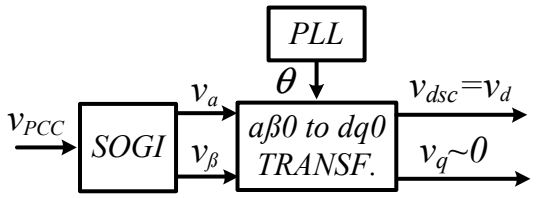

Fig. 3. DQ-frame method.

3) MSOGI-FLL Method: This method combines the SOGI orthogonal generation method with a Harmonics Decoupling Network (HDN) which isolates the different harmonics utilizing a cross-feedback network. The Simulink diagram in Fig. 4 shows how the HDN is made of summing nodes to remove all harmonics except one for each harmonic generation block. Each block includes a SOGI filter for the individual harmonics of the source voltage. This method is reported in [6] for n harmonics and it is applied here to the 3rd, 5th, 7th, 9th, 11th, and 13th harmonics. These harmonics were selected to improve the system's response to the presence of non-linear loads such as diode rectifiers, which are proliferous in consumer electronic power supplies.

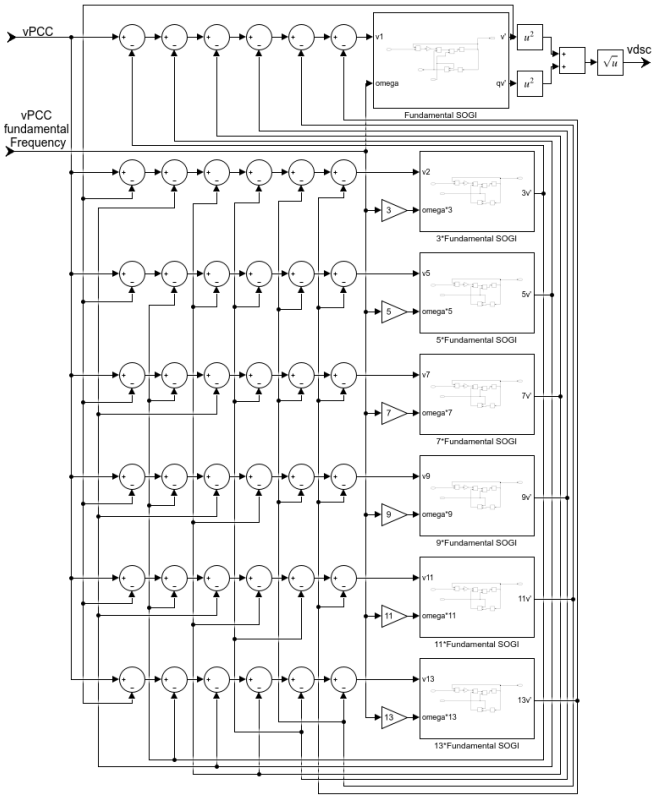

Fig. 4. Simulink implementation of the MSOGI-FLL method.

The top block, labeled "Fundamental SOGI", includes a frequency locked loop (FLL) which is used to adapt the center frequency of the SOGI as shown in Fig. 5. The FLL determines the frequency of the system and generates a sinewave in phase and a sinewave in quadrature with the input voltage. Using the SOGI shown in Fig. 5, the quadrature component (qv'), and the voltage error term (ε_v) can be used to define an equation for the frequency error term (ε_f);

$$\varepsilon_f = \varepsilon_v \cdot qv' \quad (1)$$

The average value of ε_f is positive when ω < ω' and negative for ω > ω', where ω is the input frequency of v and ω' is the estimated frequency of the FLL. By coupling the frequency error with a negative gain the FLL tracks the input frequency and thus sets the resonance frequency of the SOGI filter shown in Fig. 5 [6].

This method utilizes the filtering capability and the inherent versatility of the SOGI. The selected harmonics are fed back into the HDN to remove undesired harmonic components present in the source voltage due mostly to non-linear diode rectifier loads. In other words, the SOGI for each harmonic is fed by the grid voltage minus all the other harmonics, including the fundamental. As a result, the disconnection parameter produced by this method is significantly more sinusoidal than the distorted input voltage. This allows for much easier analysis of the input voltage by the grid disconnection algorithm. The drawback of this method is that it requires many computations.

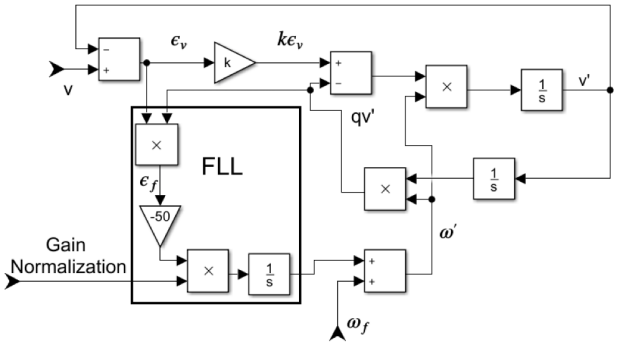

Fig. 5. Simulink implementation of the FLL used in the MSOGI-FLL method.

4) True RMS Method: This is a novel method, created to match the performance of the MSOGI-FLL method without its complexity. As shown in the block diagram of Fig. 6, a RMS calculation algorithm is used to calculate the true RMS value of the voltage at the PCC. At every time step the true RMS algorithm uses all of the samples from an entire period of the input voltage waveform.

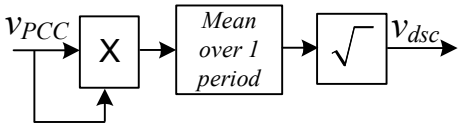

Fig. 6. True RMS method.

Each of the four methods presented above features a different "disconnection parameter", labeled v_{dsc} in Fig. 2, Fig. 3, Fig. 4 and Fig. 6, which is the control variable used by each algorithm to determine the operating state of the inverter (grid-connected or islanding mode of operation). The disconnection parameter was simulated for each method and plotted together in Fig. 7 to compare their ripple during a ride-through event. IEEE Standard 1547-2018, section 6.4.2.4.2, states: "During temporary voltage disturbances, for which the applicable voltage on the phase having the greatest voltage magnitude is greater than the maximum of the continuous

operation region, and within the corresponding voltage ranges and cumulative duration (minimum time) specified in Table 14 for abnormal operating performance Category I, Table 15 for Category II, or Table 16 for Category III, the DER shall be capable to ride-through and shall maintain synchronism with the Area EPS, shall not trip …"[1]. In this simulation we analyze higher-than normal voltages, as reported in Table II.

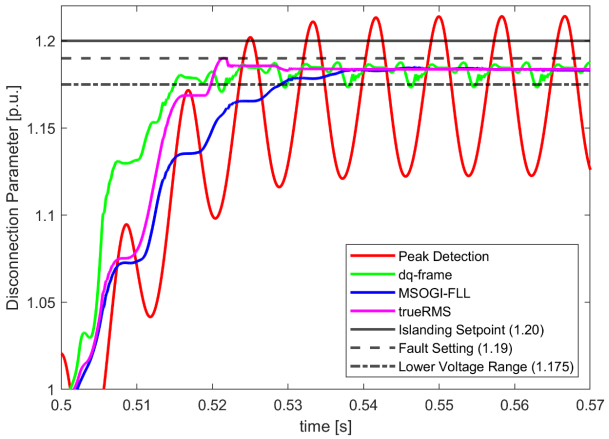

Fig. 7. Detection parameters in p.u. for the four control methods vs. IEEE Std. 1547-2018 limits.

The plots in Fig. 7 are created simulating a 1.19 p.u. over-voltage disturbance at 0.5 seconds while the DER is not intended to disconnect from the utility EPS. Furthermore, the simulation is made realistic by adding harmonics in the utility EPS voltage and a non-linear load. The non-linear load is a single-phase diode bridge rectifier, which is common in household and commercial applications. In Fig. 7 the disconnection parameters for the four methods are plotted together with the 1.19 p.u. over-voltage and the limits from [1]: the 1.20 p.u. islanding set point and the 1.175 p.u. lower voltage limit. The four methods present different peak-to-peak ripple values, which were measured from the plots in Fig. 7: 1) 0.0907 for the peak detection method, 2) 0.0146 for the dq-frame method, 3) 0.0014 for the MSOGI-FLL method, 4) about zero for the true RMS method. These peak-to-peak values are critical in meeting the requirements in IEEE Standard 1547-2018; the smaller the fluctuation of the disconnection parameter, the more accurate the controller's calculation will be of the required voltage ride-through times. If the peak-to-peak ripple of the disconnection parameter is too large, it may cause inaccurate calculations of the ride-though time or an unwanted immediate islanding condition.

Observing the plots in Fig. 7 it is clear that the peak detection method results in oscillations around the steady state value that may cause an unwanted immediate islanding condition. The dq-frame method's oscillations are not as severe as those of the peak detection method, its disconnection parameter fluctuates into a lower voltage range, which could cause an inaccurate calculation of the required ride-through time. The MSOGI-FLL method performed very well with a lower fluctuation in the disconnection parameter around the disturbance value. Finally, the true RMS method performed the best with almost zero peak-to-peak disconnection parameter ripple.

IV. Time Domain Ride-Through Simulations

In this section we report the simulated results for the MSOGI-FLL and the true RMS controllers to show their ability to meet the voltage ride-through requirements in IEEE Standard 1547-2018. These requirements proved harder to meet than the disconnection requirements.

The algorithm shown in Fig. 8 was implemented in the Simulink model to create the test conditions according to [1]. The disconnection parameter is the input to each one of the comparator blocks and the On-Off Delay blocks store the logical values generated by the comparator blocks for the required voltage ride-through time. The trip signal shown in Fig. 8 controls the mode of the inverter (grid connected or islanding mode). This algorithm was used to set up a test in which the DER inverter responds after a voltage disturbance of 0.6 p.u. occurs at 0.5 seconds.

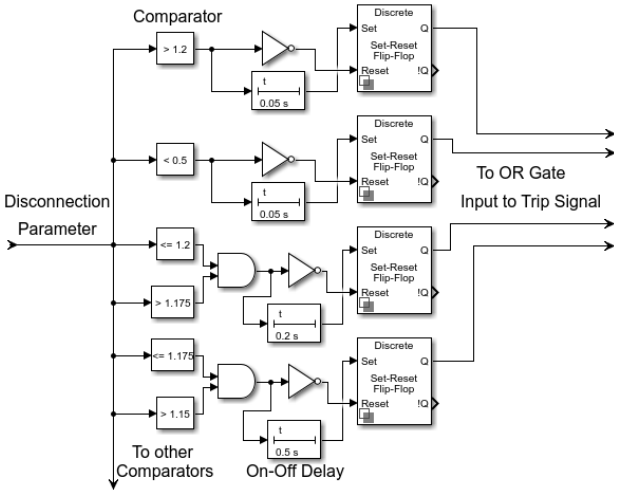

Fig. 8. Ride-through test algorithm.

Fig. 9 through Fig. 12 show the simulation results obtained when the test in Fig. 8 was performed with the MSOGI-FLL and the true RMS methods. For each method the voltage at the PCC and the disconnection parameter are plotted against the limits reported in [1], demonstrating compliance with the requirements in Table II.

In Fig. 9 and Fig. 11 a grid voltage disturbance of 0.6 p.u. is simulated at 0.5 seconds and the voltage plots demonstrate that both methods do not allow the DER inverter to island from the utility EPS for the 0.16 s required by [1]. Note that the ride –through time displayed in Fig. 9 and Fig. 11 exceeds 0.17 s, however this interval includes the time before the disturbance reaches the voltage range 0.5-0.7 p.u., which is shown in magenta in Fig. 10 and Fig. 12 for the two control methods. The "Ride-Through Difference" reported within Fig. 10 and Fig. 12 is the time it takes for the disconnection parameter to reach the voltage range; 0.5-0.7 p.u. listed in Table II. The actual ride-through time, to be checked against the value in Table II, is calculated by subtracting the "Ride-Through Difference" in Fig. 10 and Fig. 12, from the ride-through time reported in Fig. 9 and Fig. 11. These calculations result in 0.16036 s for the MSOGI-FLL method and 0.16004 with the true RMS method, which is approximately equal to the 0.16 s requirement listed in Table II.

These simulations show that both methods are viable options to implement as control strategies that meet the IEEE Standard 1547-2018 voltage ride-through requirements.

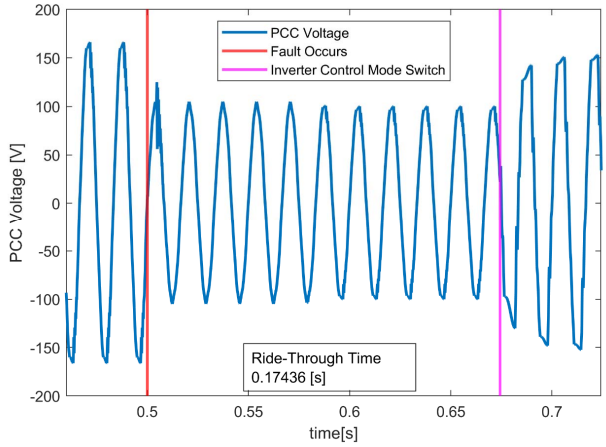

Fig. 9. PCC voltage – MSOGI-FLL method.

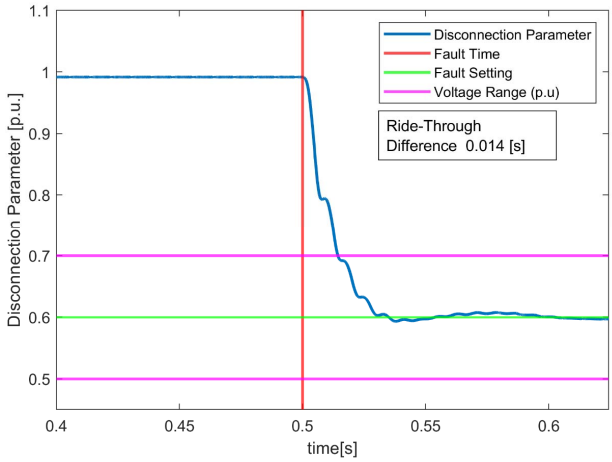

Fig. 10. MSOGI-FLL method disconnection parameter.

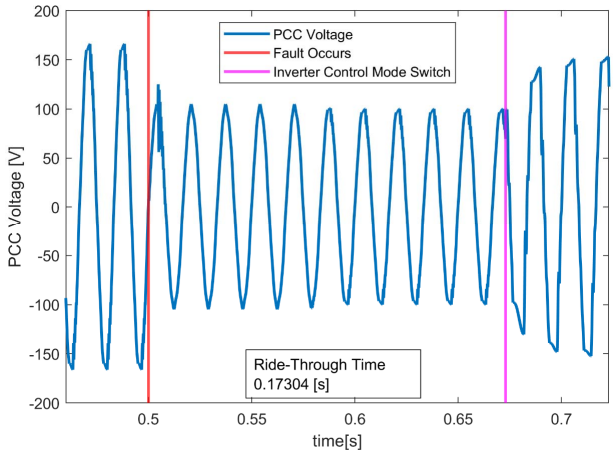

Fig. 11. PCC voltage – true RMS method.

V. Experimental Validation

The physics-based model, used for the simulations shown in the previous sections, was validated by experimental measurements performed on a laboratory prototype based on the system described in [4] where the entire control system is executed into a field programmable gate array (FPGA).

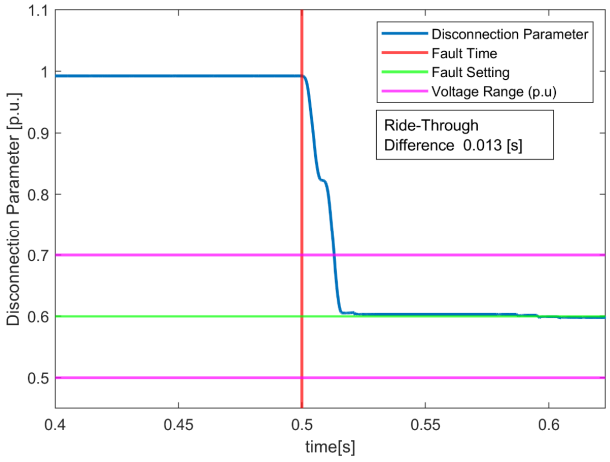

Fig. 12. True RMS method disconnection parameter.

The control method implemented in the FPGA for this experiment is the peak detection method, which is described in section III. The DER used in the laboratory is a 96V lead-acid battery pack, which interfaces the H-bridge's DC bus through a DC/DC boost converter. The DC bus voltage is regulated by the boost converter at 200V. Additional details about the experimental set-up are shown in the schematic of Fig. 13, including the load configuration. A photograph of the laboratory set-up is shown in Fig. 14.

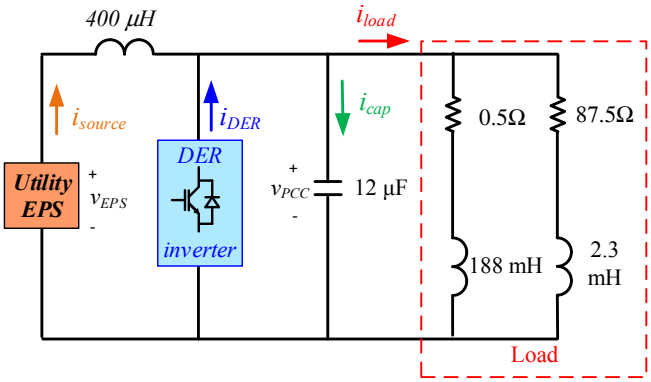

Fig. 13. Laboratory set-up for the experimental validation of the model.

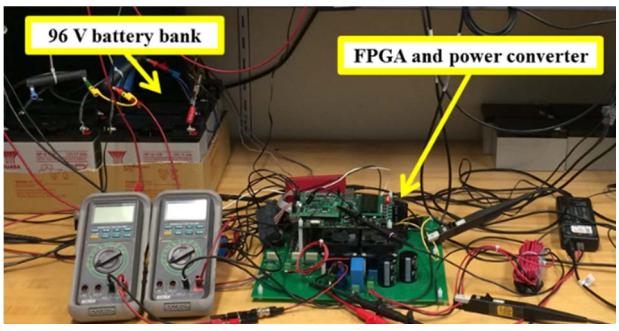

Fig. 14. Photograph of the laboratory set-up.

The physics-based model was validated with a grid-failure test performed simultaneously on the laboratory prototype and the Simulink model, to evaluate the islanding time of the inverter. The plots in Fig. 15 include simulations and experimental measurements overlaid on one another. The

waveforms show a grid failure occurring at about 0.5 s while the DER inverter was supplying 1 A of current in phase with the voltage at the point of common coupling (PCC), v_{PCC}. The grid failure was simulated by tripping the utility EPS feeder breaker in the laboratory as well as in the simulation.

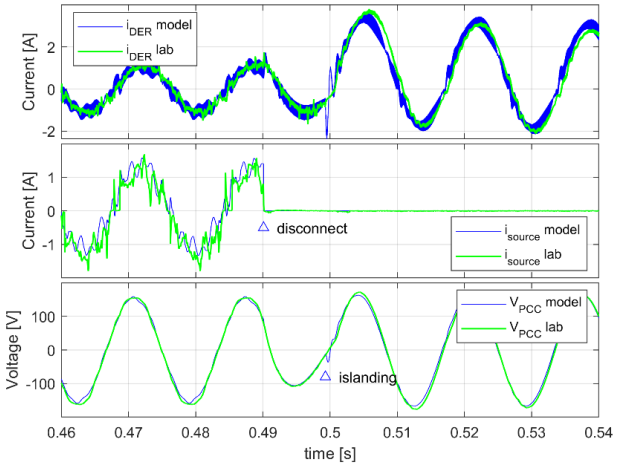

Fig. 15. Experimental validation: simulation and experimental plots for DER current, source current and PCC voltage.

The plots of the simulated and experimentally measured DER current i_{DER} , PCC voltage v_{PCC} and source current i_{source} demonstrate that the inverter picks up the load's current approximately 0.01 seconds after the loss of utility EPS. The transition to islanding mode is smaller than a 60Hz cycle and meets the limits in [1] by a large margin. The maximum transition time set by IEEE Standard 1547-2018 is 0.16 s, which is 10x 60Hz cycles. It is interesting to note that this excellent performance is obtained with the simplest of the methods evaluated in this paper, the peak detection method, described in the next section. The simulated and experimental waveforms in Fig. 15 are very similar, demonstrating the accuracy of the physics-based model. This experiment validates the physics-based model which was used to compare the ride-through performance of the different control methods in the previous sections.

VI. Conclusions

This paper compares different controllers for a single-phase inverter interfacing a DER to determine its operating mode when there are voltage abnormalities at the point of common coupling. IEEE Standard 1547-2018 provides guidance on when a DER should ride-through such abnormal conditions and when it should disconnect from the area EPS, thus going into islanding-mode of operation [1].

In this research we show that, while disconnect times are quite easy to achieve, the voltage ride-through requirements are challenging. In particular, it is difficult to adhere to the standard when the voltage being measured is highly distorted, as in the experiments presented in this paper. This situation is more common in today's electrical environment where non-linear loads are ever more prevalent in household electronics and industry.

The experiments reported in section V demonstrate that if a fault occurs that requires an immediate islanding condition (0.50 p.u. or 1.20 p.u.) the 0.16 s response time is easily accomplished even by the simplest controller. However more accurate control methods are required to meet the ride-through requirements in [1]. Ultimately, the two control structures implemented in the time-domain ride-through simulation were chosen because of their accuracy following a transient in the presence of non-linear loads such as diode rectifier. Of the four control strategies presented in this paper the novel true RMS method is the simplest to implement and allows adherence to IEEE Standard 1547-2018.

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